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Image AF/2827

| TRANSMITTAL LETTER (General - Patent Pending) | Docket No. 121056-020 |
|---|---|

Re Application Of: **Hiroshi KIMURA**

| Serial No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| 09/837,022 | April 18, 2001 | James Mitchell | 2827 |

Title:

**SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD AND ELECTRO DEPOSITION FRAME**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is:

**Brief on Appeal (one original and two copies)**
**Brief Transmittal**
**Fee Transmittal**

in the above identified application.

- ☐ No additional fee is required.
- ☐ A check in the amount of is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **12-2136** as described below.
  - ☒ Charge the amount of **$330.00**
  - ☒ Credit any overpayment.
  - ☒ Charge any additional fee required.

Michael S. Gzybowski

*Signature*

Dated: **January 30, 2004**

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Michael S. Gzybowski

*Signature of Person Mailing Correspondence*

**Michael S. Gzybowski**

*Typed or Printed Name of Person Mailing Correspondence*

cc:

PTO/SB/17 (08-03)
Approved for use through 07/31/2006. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE


# FEE TRANSMITTAL for FY 2003

*Effective 01/01/2003. Patent fees are subject to annual revision.*

☐ Applicant claims small entity status. See 37 CFR 1.27

**TOTAL AMOUNT OF PAYMENT** ($) **$330.00**

| *Complete if Known* | |
|---|---|
| Application Number | 09/837,022 |
| Filing Date | April 18, 2001 |
| First Named Inventor | Hiroshi KIMURA |
| Examiner Name | James Mitchell |
| Art Unit | 2827 |
| Attorney Docket No. | 121056-020 |

## METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 12-2136

Deposit Account Name: BUTZEL LONG

**The Director is authorized to:** *(check all that apply)*

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additonal fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1001 | 750 | 2001 | 375 | Utility filing fee | |
| 1002 | 330 | 2002 | 165 | Design filing | |
| 1003 | 520 | 2003 | 260 | Plant filing fee | |
| 1004 | 750 | 2004 | 375 | Reissue filing | |
| 1005 | 160 | 2005 | 80 | Provisional filing fee | |

SUBTOTAL (1) ($)

### 2. EXTRA CLAIM FEES FOR UTILITY AND

| | Extra Claims | | Fee from below | Fee Paid |
|---|---|---|---|---|
| Total Claims | -20** = 0 | X | | = 0.00 |
| Independent Claims | - 3** = 0 | X | | = 0.00 |
| Multiple Dependent | | | | = |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 84 | 2201 | 42 | Independent claims in excess of 3 |
| 1203 | 280 | 2203 | 140 | Multiple dependent claim, if not paid |
| 1204 | 84 | 2204 | 42 | ** Reissue independent claims over original patent |
| 1205 | 18 | 2205 | 9 | ** Reissue claims in excess of 20 and over original patent |

SUBTOTAL (2) ($) **$0.00**

***or number previously paid, if greater; For Reissues, see above*

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge - late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge - late provisional filing fee or cover sheet | |
| 1053 | 130 | 1053 | 130 | Non - English specification | |
| 1812 | 2,520 | 1812 | 2,520 | For filing a request for *ex parte* reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1,840* | 1805 | 1,840* | Requesting publication of SIR after Examiner action | |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | |
| 1252 | 410 | 2252 | 205 | Extension for reply within second month | |
| 1253 | 930 | 2253 | 465 | Extension for reply within third month | |
| 1254 | 1,450 | 2254 | 725 | Extension for reply within fourth month | |
| 1255 | 1,970 | 2255 | 985 | Extension for reply within fifth month | |
| 1401 | 320 | 2401 | 160 | Notice of Appeal | |
| 1402 | 320 | 2402 | 160 | Filing a brief in support of an appeal | 330.00 |
| 1403 | 280 | 2403 | 140 | Request for oral hearing | |
| 1451 | 1,510 | 1451 | 1,510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive - unavoidable | |
| 1453 | 1,300 | 2453 | 650 | Petition to revive - unintentional | |
| 1501 | 1,300 | 2501 | 650 | Utility issue fee (or reissue) | |
| 1502 | 470 | 2502 | 235 | Design issue fee | |
| 1503 | 630 | 2503 | 315 | Plant issue fee | |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | |
| 1807 | 50 | 1807 | 50 | Processing fee under 37 CFR § 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of Information Disclosure Statement | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 750 | 2809 | 375 | Filing a submission after final rejection (37 CFR § 1.129(a)) | |
| 1810 | 750 | 2810 | 375 | For each additional invention to be examined (37 CFR § 1.129(b)) | |
| 1801 | 750 | 2801 | 375 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) **$330.00**

## SUBMITTED BY

Complete *(if applicable)*

| Name (Print/Type) | Michael S. Gzybowski | Registration No. (Attorney/Agent) | 32,816 | Telephone | 734-995-3110 |
|---|---|---|---|---|---|
| Signature | Michael S Gzybowski | | | Date | January 30, 2004 |

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PATENT APPLICATION

*IN THE UNITED STATES PATENT AND TRADEMARK OFFICE*

| | |
|---|---|
| *Group Art Unit:* | 2827 |
| *Attorney Docket No.:* | 121056-020 |
| *Applicant:* | Hiroshi KIMURA |
| *Invention:* | SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD AND ELECTRO DEPOSITION FRAME |
| *Serial No:* | 09/837,022 |
| *Filed:* | April 18, 2001 |
| *Examiner:* | James Mitchell |

Certificate Under 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

on January 30, 2004

Michael S. Gzybowski

## BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to Appellant's Notice of Appeal filed December 1, 2003 in connection with the above-identified application, appellant submits the present Brief on Appeal.

## REAL PARTY IN INTEREST

Appellant has assigned this application to Torex Semiconductor Ltd. in an assignment which was executed by the inventor on April 11, 2001, and filed in the United States Patent and

Trademark Office on April 18, 2001, and recorded on April 18, 2001 at Reel No. 012012 and Frame No. 0420.

## RELATED APPEALS AND INTERFERENCES

There are no related cases involved in any appeal procedures or Interferences.

## STATUS OF CLAIMS

Claims 5-8 are pending in this application. Claims 5-8 stand under Final Rejection, from which rejection of claims 5-8 this appeal is taken. No other claims are pending.

## STATUS OF AMENDMENTS

An Amendment Final Rejection was filed in the application of December 18, 2003 which corrected a minor typographical error in claim 5. To date, appellant has not received a response from the Patent and Trademark Office; however, it is assumed that the Amendment After Final will be entered.

## SUMMARY OF INVENTION

The present invention is directed to a method of manufacturing a semiconductor device that involves first forming an electrodeposition frame on a flexible flat metallic substrate. The

manner in which the electrodeposition frame is formed is detailed in first two steps of the process depicted in Figs. 4A – 4B and discussed from the first paragraph on page 13 of appellant's specification through the first paragraph on page 14 of appellant's specification.

As noted, the electrodeposition frame has second metallic layers 8a and first metallic layers 8a for external extension being patterned, wherein the first metallic layers 8b are thicker than said second metallic layers 8a.

After the electrodeposition frame is formed a plurality of semiconductor elements 2 having electrode pads thereon are contiguously mounted on the metallic layers 8b as detailed in the third step of the process depicted in Fig. 4C and discussed in the last full paragraph on page 14 of appellant's specification

After the semiconductor elements 2 are mounted on the metallic layers 8b, the electro pads of the semiconductor elements 2 are wire-bonded to the metallic layers 8a which are located between the semiconductor elements as depicted in Fig. 4E and discussed in the paragraph bridging pages 14 and 15 of appellant's specification.

After the semiconductors have been wire-bonded, the semiconductor elements mounted on said electrodeposition frame are resin-sealed or molded as discussed in the first three full paragraphs on page 15 of appellant's specification.

After the resin-sealing/molding step, the metallic substrate is removed to provide a resin sealing body having a bottom so that rear surfaces of the metallic layers 8b and metallic layers 8a are flush with the bottom of the resin sealing body as depicted in Fig. 5B and discussed in the paragraph bridging pages 15 and 16 of appellant's specification.

In the next step in the process which is discussed from the first full paragraph on page 16 through the paragraph bridging pages 16 and 17 of appellant's specification, the resin

sealing body is cut into individual semiconductor devices, wherein each device is provided with the first and second metallic layers 8b and 8a.

In a final step of the process which is discussed in the second full paragraph on page 17 of appellant's specification metallic thin films are deposited on portions of the first and second metallic layers 8b and 8a that are exposed at the bottom the resin sealing body.

## ISSUE

Whether claims 5, 6 and 8 are unpatentable over Glenn in combination with Jung et al. and Kweon et al. under 35 U.S.C. §103(a).

Whether claim 7 is unpatentable over Glenn in combination with Jung et al. and Matsushita under 35 U.S.C. §103(a).

## GROUPING OF CLAIMS

Claims 5, 6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn in combination with Jung et al. and Kweon et al. and therefore stand or fall together under this rejection.

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn in combination with Jung et al. and Matsushita and therefore stand or fall together separately from claims 5, 6 and 8 under this rejection.

## THE REFERENCES

The following references are relied upon by the examiner:

| | | |
|---|---|---|
| U.S. 2002/0100165 | Glenn | Aug. 1, 2002 |
| U.S. 6,333,252 | Jung et al. | Dec. 25, 2001 |
| U.S. 5,900,676 | Kweon et al. | May 4, 1999 |
| JP 2001-024001 | Matsushita | Jan. 26, 2001 |

## BRIEF DESCRIPTION OF THE REFERENCES

Glenn discloses a method of forming an integrated circuit device package that utilizes a temporary substrate which substrate is an "inexpensive plastic sheet" that serves as "a base for forming the packages."

Glenn specifically notes disadvantages in the art that are directly associated with using a "metal temporary substrate and low-melting point alloy layer." Such advantages are discussed in paragraphs 0004 and 0006, and the solution thereof is mentioned in paragraphs 0007 and 0010 of Glenn.

Glenn expressly teaches against the use of metallic substrates and exemplifies plastic tape such as KAPTON polyimide tape from Dupont Company as a suitable substrate.

Jung et al. discloses a low-pin-count chip package and a method of making the same which requires the use of a metal substrate 260 (Fig. 3) upon which the chip package is formed. Jung et al. teaches that after formation of the chip package, the metal substrate 260 is removed by an etching process (Column 4, lines 26-32).

Kweon et al. discloses a semiconductor device package having column leads and a method of making the same which involves the initial steps forming an polyimide film on a column lead material and etching the column lead material to form a plurality of column leads 24 and a die pad 22. (See Figs. 1-3). In a final step the polyimide film 30 and metal layer 40 are removed simultaneously.

Matsushita discloses a manufacture of resin-encapsulated semiconductor devices and lead frames that utilizes a sealing sheet 6 that is placed between a metal mold plane and the backsheet of the lead frame 4.

## THE REJECTIONS

Claims 5, 6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn in combination with Jung et al. and Kweon et al.

Under this rejection the examiner has relied upon Glenn as disclosing:

> a method of manufacturing a plurality of semiconductor devices comprising steps of forming an electrodeposition frame (via etched metal; Par. 0037, 0038, Line 1) on a flexible substrate (10), said electrodeposition frame having first metallic layers (20) and second metallic layers (24) for external extension being patterned, wherein the first metallic layers are thicker than said second metallic layers so that the rear surfaces of the first and second metallic layers are flush with the bottom of the resin, contiguously mounting a semiconductor (28) with inherent electrode pads thereon said first metallic layers, wire bonding (29) the electrode pads to said second metallic layers, resin-sealing (30) said semiconductor element mounted on said electrodeposition frame is resin sealed with said semiconductor and using the substrate as a lower die, removing said substrate (Par 0053) to provide a resin sealing body; cutting said second metallic layers (Fig. 11, 13) and cutting a resin sealing body into individual semiconductor devices (Par 0056).

The Examiner concedes that "Glenn does not appear to disclose that said substrate is a metallic flexible substrate..."

The Examiner has accordingly relied upon Jung et al. as utilizing "an inherently flexible metallic substrate (260)."

In combining the teachings of Glenn and Jung et al. the Examiner takes the position that:

> It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

In addition the Examiner states that:

> Furthermore, it would have been obvious....to use metallic substrate as an alternate temporary substrate since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416 (1960).

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn and Jung et al and further in view of Matsushita.

Under this rejection the examiner has relied upon Matsushita as disclosing cutting through a sealing resin and a centerline of second metallic layers.

In combining the teachings of Glenn, Jung et al. and Matsushita the Examiner takes the position that:

> It would have been obvious....to modify the manufacturing process by the number of leads etched in Glenn, such that each lead is attached to two dies and then the sealing resin and a center line of each second metallic layer is cut in order to reduce cutting process time as taught by Matsushita.

## ARGUMENT

Appellant respectfully urges that claims 5, 6 and 8 patentably distinguish from the applied reference combination as the claimed subject matter would not have been obvious within the meaning of 35 U.S.C. §103(a).

In determining obviousness, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." (*Grain Processing v. American Maize*, 5 USPQ 2d 1788, 1793 (Fed. Cir. 1988))

In the present situation, it is submitted that rather than the combination of the prior art rendering obvious appellant's claimed invention as the Examiner purports, the prior art actually teaches against the manner in which the Examiner proposes to combine the teachings of the prior art.

It is submitted that if any of the references relied upon support a rejection under 35 U.S.C. §103 teach against the proposed modification, the prior art cannot "make obvious the invention," particularly when the proposed modification goes against the express teachings of the primary reference which is being modified.

While an Examiner can and should rely upon what the teachings of the references suggest, the Examiner cannot overlook or exclude from consideration what the references teach against.

If the proposed combination or modification destroys the teachings of one of the references relied upon, the combination is clearly improper. (See *Ex parte Hartmann*, 186 USPQ 366 (PTO Bd App 1974).

The Examiner has relied upon Glenn as disclosing:

> ...a method of manufacturing a plurality of semiconductor devices comprising steps of forming an electrodeposition frame (via etched metal; Par. 0037, 0038, Line 1) on a flexible substrate (10), said electrodeposition frame having first metallic layers (20) and second metallic layers (24) for external extension being patterned, wherein the first metallic layers are thicker than said second metallic layers so that the rear surfaces of the first and second metallic layers are flush with the bottom of the resin, contiguously mounting a semiconductor (28) with inherent electrode pads thereon said first metallic layers, wire bonding (29) the electrode pads to said second metallic layers, resin-sealing (30) said semiconductor element mounted on said electrodeposition frame is resin sealed with said semiconductor and using the substrate as a lower die, removing said substrate (Par 0053) to provide a resin sealing body; cutting said second metallic layers (Fig. 11, 13) and cutting a resin sealing body into individual semiconductor devices (Par 0056).

The Examiner concedes that "Glenn does not appear to disclose that said substrate is a metallic flexible substrate..." (emphasis added).

The Examiner has accordingly relied upon Jung et al. as utilizing "an inherently flexible metallic substrate (260)." (emphasis added).

In combining the teachings of Glenn and Jung et al. the Examiner takes the position that:

> It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

In addition the Examiner states that:

> Furthermore, it would have been obvious....to use metallic substrate as an alternate temporary substrate since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416 (1960).

It is important to fully consider the teachings of Glenn.

In paragraph 0004 Glenn introduces the invention in the context of disadvantages associated with the prior art by pointing out that the prior art has:

> ...foreseeable disadvantages. For example, the use of the metal temporary substrate and low-melting point alloy layer increase costs and manufacturing difficulty.

Thus, according to the teachings of Glenn, the prior art use of metallic substrates are associated with disadvantages that Glenn is concerned about overcoming and avoiding.

In paragraph 0006 Glenn discusses further disadvantages with the prior art stating:

> First, the use of acid to dissolve the remainder of the copper plate after encapsulation creates a significant possibility of contamination, since such acids are generally regarded as dirty.

Again, Glenn indicates that the prior art use of metallic substrates requires the substrates to be removed by etching processes which produce contaminates that can adversely effect the resulting semiconductor devices.

In paragraph 0007 Glenn teaches that:

> Accordingly, there is a need for a small and reliable package that is easier and less expensive to manufacture than prior art packages.

In paragraph 0010 Glenn teaches:

> The present invention overcomes the disadvantages of the prior art by, among other things, the use of an inexpensive plastic sheet as a base for forming the packages

As a solution to the prior art use of metallic substrates and their associated disadvantages, Glenn purposely utilizes a plastic substrate having an adhesive surface which is exemplified by the use of adhesive tape in paragraph 0008.

The use of such a substrate allows Glenn to achieve a lower cost and a method of removing the substrate without exposing the packaged semiconductor device to potentially harmful etching solutions which are required to remove metallic substrates in the prior art.

It is accordingly submitted that Glenn's invention is directed to the use of a plastic substrate and the exclusion of metallic substrates in order to overcome the noted disadvantages of a metallic substrate.

The Examiner has conceded that Glenn fails to teach a metallic substrate.

Accordingly, the Examiner has relied upon Jung et al. as teaching the use of a metallic substrate 260.

As taught by Jung et al., substrate 260 is removed at the end of the fabrication process "utilizing an etching agent."

It is submitted that it would go against the express teachings of Glenn to modify Glenn to include the metallic substrate of Jung et al. as the Examiner suggests.

First, it is pointed out that the Examiner's proposed combination of Glenn and Jung et al. is improper under U.S. Patent Law because it is completely contrary to the express teachings of Glenn.

As held by the Patent Office Board of Appeals and Interferences in *Ex parte Hartmann*:

> References cannot properly be combined if effect would destroy invention on which one of reference patents is based. *Ex parte Hartmann*, 186 USPQ 366 (PTO Bd App 1974).

In response to the Examiner's stated basis that:

> It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

It is noted that Glenn teaches advantages associated with utilizing a plastic substrate over a metallic substrate.

Accordingly, plastic and metallic substrates cannot be considered equivalents or alternatives in the present situation. Glenn's choice of plastic substrates is not arbitrary, but rather based upon concrete disadvantages associated with metallic substrates and advantages associated with plastic substrates.

As held by the court of appeals in *In re Wesslau*:

> It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. *In re Wesslau*, 147 USPQ 391 (CCPA 1965).

Under this holding, the Examiner is required to fully consider the reasons as to why Glenn utilizes a plastic substrate and avoids the use of a metallic substrate.

When fully considering the teachings of Glenn, it becomes "obvious" that Glenn expressly avoids the use of a metallic substrate.

Accordingly, the express teachings of Glenn do not support the Examiner's position that:

> It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

The Examiner's second basis for modifying Glenn in view of Jung et al. was stated as follows:

> Furthermore, it would have been obvious....to use metallic substrate as an alternate temporary substrate since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416 (1960).

*In re Leshin* involves a situation in which the Board of Patent Appeals and Interferences upheld a rejection on the basis that:

> ...mere selection of known plastics to make container-dispenser of a type made of plastics prior to the invention, the selection of the plastics being on basis of suitability for intended use, is obvious.

In *In re Leshin* the prior art taught various plastic materials and the appellant argued that he "had to select them for his particular purpose" after conceding that the "the plastics he uses are well known"

In the present situation the Examiner is trying to apply the holding of *In re Leshin* to a situation in which the primary reference teaches a plastic substrate in order to overcome disadvantages associated with the prior art use of metallic substrates, and the secondary reference teaches a metallic substrate.

This is not a case of selective use of similar materials as in the case of *In re Leshin*. Moreover, Glenn expressly teaches functional differences and disadvantages associated with metallic substrates verses plastic substrates.

Therefore the holding in *In re Leshin* does not support the Examiners' stated position on obviousness and the Examiner's second basis for concluding that appellant's claimed invention is obvious over Glenn in view of Jung et al. is unfounded.

It is noted that in Glenn the lead frame and plastic substrate are attached to each other by an adhesive material. However, after attachment, peeling may occur which would allow the sealing resin to seep in between the lead frame and the plastic substrate. In such a case, the seeped in sealing resin cannot be removed and therefore poor conductivity may occur.

In contrast to Glenn, in the present invention the Ni (metallic layer) is formed by electrodeposition so that no gap is formed between the Ni layer and SUS. Therefore, the sealing resin cannot seep in between the Ni layer and SUS.

In Glenn the problem of the sealing resin seeping between the lead frame and plastic substrate can only be achieved by increasing the adhesive strength of the polyimide adhesive tape. This causes additional problems because after the plastic substrate is removed, the additional adhesive must also be removed. This adds an additional process step and increases costs.

The Examiner has relied upon Kweon et al. as teaching the use of deposited metallic thin film portions on first and second metallic layers that are exposed from a rear surface of a resin body.

In combining the teachings of Kweon et al. with those of Glenn and Jung et al. the Examiner states that:

> It would have been obvious....to deposit thin film portions of the first and second metallic payers that are exposed from a rear surface of said resin sealing body in order to provide electrical and mechanical connection as taught by Kweon.

The Examiner's further reliance upon Kweon et al. does not overcome the fact that the combination of Glenn and Jung et al. is improper under 35 U.S.C. §103.

The Examiner has relied upon Matsushita as disclosing cutting through a sealing resin and a centerline of second metallic layers.

The Examiner's further reliance upon Matsushita does not overcome the fact that the combination of Glenn and Jung et al. is improper under 35 U.S.C. §103.

In the Advisory Action of November 11, 2003 the Examiner has stated that:

> ...applicant has not provided extrinsic evidence that replacing the substrate of Glenn with another material will destroy the invention.

In response to the Examiner's position and suggestion for appellant to submit extrinsic evidence, a Declaration by Mr. KIMURA (unsigned) was being submitted under the provisions of 37 CFR §1.132.

The KIMURA Declaration provides a technical explanation from someone who is qualified as having ordinary skill in the art, as to the differences between applying metal layers on metal and plastic substrates and electrodeposition techniques for fabricating semiconductor devices.

The technical facts set forth in the KIMURA Declaration support appellant's position that it would not have been obvious to modify Glenn in a manner which involves substituting the plastic substrate of Glenn for the metal substrate of Jung et al.

From the facts in the KIMURA Declaration considered in light of the teachings of Glenn, one skilled in the art can readily conclude that Glenn does not teach electrodeposition at all, let alone forming an electrodeposition frame on a metal substrate.

Rather, Glenn teaches that "metal layer 16 may be applied by sputtering or chemical vapor deposition."

Moreover, Glenn does not recognize or appreciate, or is in any concerned with the differences in contact strength between metal layers on plastic substrates (deposited by sputtering or CVD techniques) and metal layers electrodeposited on metal substrates as explained in the KIMURA Declaration.

The Examiner's combination of the prior art is based upon the premise that there is no difference between using a plastic substrate in Glenn or modifying Glenn to have a metal substrate.

It is submitted that the facts in the KIMURA Declaration establish that there are significant differences between using a plastic substrate and a metal substrate in the fabrication of semiconductor devices.

Accordingly, it is submitted that the record, including the teachings of the prior art and the KIMURA Declaration, support appellant's position that the combination of Glenn and Jung et al. is not obvious under 35 U.S.C. §103, and that appellant's claimed invention is patentably distinguishable over the prior art.

It is noted that a signed copy of the KIMURA declaration will not be available until the second week of February. Accordingly, consideration of the technical facts presented in the KIMURA declaration is requested while arrangements are being made to submit a signed copy of the KIMURA declaration.

## CONCLUSION

For the reasons advanced above, appellant respectfully contends that the rejection of claims 5, 6 and 8 as being obvious under 35 U.S.C. §103(a) over Glenn. in view of Jung et al. and Kweon is improper because the examiner has not met the burden of establishing a *prima facie* case of obviousness.

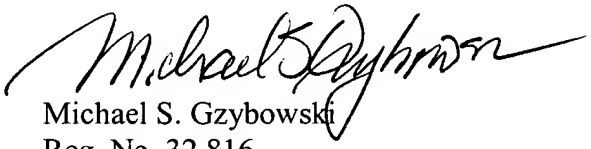
Moreover, for the reasons advanced above, appellant respectfully contends that the rejection of claim 7 as being obvious under 35 U.S.C. §103(a) over Glenn and Jung et al. and

further in view of Matsushita is improper because the examiner has not met the burden of establishing a *prima facie* case of obviousness.

Reversal of each of the rejections on appeal is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 CFR §1.136 is hereby made. Please charge the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 12-2136 and please credit any excess fees to such deposit account.

Respectfully submitted,



Michael S. Gzybowski
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## CLAIMS ON APPEAL

Claim 5. A method of manufacturing a semiconductor device comprising the steps of:

forming an electrodeposition frame on a flexible flat metallic substrate, said electrodeposition frame having first metallic layers and second metallic layers for external extension being patterned, wherein said first metallic layers are thicker than said second metallic layers;

contiguously mounting a plurality of semiconductor elements, each with electrode pads thereon, on said first metallic layers;

wire-bonding the electrode pads to said second metallic layers which are located between said semiconductor elements;

resin-sealing said semiconductor elements mounted on said electrodeposition frame;

removing said metallic substrate to provide a resin sealing body having a bottom so that rear surfaces of the first metallic layers and second metallic layers are flush with the bottom of said resin sealing body;

cutting said resin sealing body into individual semiconductor devices, wherein each device is provided with the first and second metallic layers; and

depositing metallic thin films on portions of the first and second metallic layers that are exposed at the bottom said resin sealing body.

Claim 6 A method of manufacturing a semiconductor device according to claim 5, further comprising after the step of cutting, the step of:

depositing metallic layers for electrodes to the second metallic layers exposed from a rear surface of said resin sealing body.

Claim 7 A method of manufacturing a semiconductor device according to claim 5, wherein

in said step of cutting of said resin sealing body, it is cut along a center line of each of the second metallic layers to provide metallic layers for external extension for adjacent semiconductor elements.

Claim 8 A method of manufacturing a semiconductor device according to claim 5, wherein said electrodeposition frame is resin sealed together with said semiconductor elements using said metallic substrate as a lower die.

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PATENT APPLICATION

*IN THE UNITED STATES PATENT AND TRADEMARK OFFICE*

| | |
|---|---|
| *Group Art Unit:* | 2827 |
| *Attorney Docket No.:* | 121056-020 |
| *Applicant:* | Hiroshi KIMURA |
| *Invention:* | SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD AND ELECTRO DEPOSITION FRAME |
| *Serial No:* | 09/837,022 |
| *Filed:* | April 18, 2001 |
| *Examiner:* | James Mitchell |

Certificate Under 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

on January 30, 2004

Michael S. Gzybowski

## BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to Appellant's Notice of Appeal filed December 1, 2003 in connection with the above-identified application, appellant submits the present Brief on Appeal.

## REAL PARTY IN INTEREST

Appellant has assigned this application to Torex Semiconductor Ltd. in an assignment which was executed by the inventor on April 11, 2001, and filed in the United States Patent and

Trademark Office on April 18, 2001, and recorded on April 18, 2001 at Reel No. 012012 and Frame No. 0420.

## RELATED APPEALS AND INTERFERENCES

There are no related cases involved in any appeal procedures or Interferences.

## STATUS OF CLAIMS

Claims 5-8 are pending in this application. Claims 5-8 stand under Final Rejection, from which rejection of claims 5-8 this appeal is taken. No other claims are pending.

## STATUS OF AMENDMENTS

An Amendment Final Rejection was filed in the application of December 18, 2003 which corrected a minor typographical error in claim 5. To date, appellant has not received a response from the Patent and Trademark Office; however, it is assumed that the Amendment After Final will be entered.

## SUMMARY OF INVENTION

The present invention is directed to a method of manufacturing a semiconductor device that involves first forming an electrodeposition frame on a flexible flat metallic substrate. The

manner in which the electrodeposition frame is formed is detailed in first two steps of the process depicted in Figs. 4A – 4B and discussed from the first paragraph on page 13 of appellant's specification through the first paragraph on page 14 of appellant's specification.

As noted, the electrodeposition frame has second metallic layers 8a and first metallic layers 8a for external extension being patterned, wherein the first metallic layers 8b are thicker than said second metallic layers 8a.

After the electrodeposition frame is formed a plurality of semiconductor elements 2 having electrode pads thereon are contiguously mounted on the metallic layers 8b as detailed in the third step of the process depicted in Fig. 4C and discussed in the last full paragraph on page 14 of appellant's specification

After the semiconductor elements 2 are mounted on the metallic layers 8b, the electro pads of the semiconductor elements 2 are wire-bonded to the metallic layers 8a which are located between the semiconductor elements as depicted in Fig. 4E and discussed in the paragraph bridging pages 14 and 15 of appellant's specification.

After the semiconductors have been wire-bonded, the semiconductor elements mounted on said electrodeposition frame are resin-sealed or molded as discussed in the first three full paragraphs on page 15 of appellant's specification.

After the resin-sealing/molding step, the metallic substrate is removed to provide a resin sealing body having a bottom so that rear surfaces of the metallic layers 8b and metallic layers 8a are flush with the bottom of the resin sealing body as depicted in Fig. 5B and discussed in the paragraph bridging pages 15 and 16 of appellant's specification.

In the next step in the process which is discussed from the first full paragraph on page 16 through the paragraph bridging pages 16 and 17 of appellant's specification, the resin

sealing body is cut into individual semiconductor devices, wherein each device is provided with the first and second metallic layers 8b and 8a.

In a final step of the process which is discussed in the second full paragraph on page 17 of appellant's specification metallic thin films are deposited on portions of the first and second metallic layers 8b and 8a that are exposed at the bottom the resin sealing body.

## ISSUE

Whether claims 5, 6 and 8 are unpatentable over Glenn in combination with Jung et al. and Kweon et al. under 35 U.S.C. §103(a).

Whether claim 7 is unpatentable over Glenn in combination with Jung et al. and Matsushita under 35 U.S.C. §103(a).

## GROUPING OF CLAIMS

Claims 5, 6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn in combination with Jung et al. and Kweon et al. and therefore stand or fall together under this rejection.

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn in combination with Jung et al. and Matsushita and therefore stand or fall together separately from claims 5, 6 and 8 under this rejection.

## THE REFERENCES

The following references are relied upon by the examiner:

| | | |
|---|---|---|
| U.S. 2002/0100165 | Glenn | Aug. 1, 2002 |
| U.S. 6,333,252 | Jung et al. | Dec. 25, 2001 |
| U.S. 5,900,676 | Kweon et al. | May 4, 1999 |
| JP 2001-024001 | Matsushita | Jan. 26, 2001 |

## BRIEF DESCRIPTION OF THE REFERENCES

Glenn discloses a method of forming an integrated circuit device package that utilizes a temporary substrate which substrate is an "inexpensive plastic sheet" that serves as "a base for forming the packages."

Glenn specifically notes disadvantages in the art that are directly associated with using a "metal temporary substrate and low-melting point alloy layer." Such advantages are discussed in paragraphs 0004 and 0006, and the solution thereof is mentioned in paragraphs 0007 and 0010 of Glenn.

Glenn expressly teaches against the use of metallic substrates and exemplifies plastic tape such as KAPTON polyimide tape from Dupont Company as a suitable substrate.

Jung et al. discloses a low-pin-count chip package and a method of making the same which requires the use of a metal substrate 260 (Fig. 3) upon which the chip package is formed. Jung et al. teaches that after formation of the chip package, the metal substrate 260 is removed by an etching process (Column 4, lines 26-32).

Kweon et al. discloses a semiconductor device package having column leads and a method of making the same which involves the initial steps forming an polyimide film on a column lead material and etching the column lead material to form a plurality of column leads 24 and a die pad 22. (See Figs. 1-3). In a final step the polyimide film 30 and metal layer 40 are removed simultaneously.

Matsushita discloses a manufacture of resin-encapsulated semiconductor devices and lead frames that utilizes a sealing sheet 6 that is placed between a metal mold plane and the backsheet of the lead frame 4.

## THE REJECTIONS

Claims 5, 6 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn in combination with Jung et al. and Kweon et al.

Under this rejection the examiner has relied upon Glenn as disclosing:

> a method of manufacturing a plurality of semiconductor devices comprising steps of forming an electrodeposition frame (via etched metal; Par. 0037, 0038, Line 1) on a flexible substrate (10), said electrodeposition frame having first metallic layers (20) and second metallic layers (24) for external extension being patterned, wherein the first metallic layers are thicker than said second metallic layers so that the rear surfaces of the first and second metallic layers are flush with the bottom of the resin, contiguously mounting a semiconductor (28) with inherent electrode pads thereon said first metallic layers, wire bonding (29) the electrode pads to said second metallic layers, resin-sealing (30) said semiconductor element mounted on said electrodeposition frame is resin sealed with said semiconductor and using the substrate as a lower die, removing said substrate (Par 0053) to provide a resin sealing body; cutting said second metallic layers (Fig. 11, 13) and cutting a resin sealing body into individual semiconductor devices (Par 0056).

The Examiner concedes that "Glenn does not appear to disclose that said substrate is a metallic flexible substrate..."

The Examiner has accordingly relied upon Jung et al. as utilizing "an inherently flexible metallic substrate (260)."

In combining the teachings of Glenn and Jung et al. the Examiner takes the position that:

> It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

In addition the Examiner states that:

> Furthermore, it would have been obvious....to use metallic substrate as an alternate temporary substrate since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416 (1960).

Claim 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Glenn and Jung et al and further in view of Matsushita.

Under this rejection the examiner has relied upon Matsushita as disclosing cutting through a sealing resin and a centerline of second metallic layers.

In combining the teachings of Glenn, Jung et al. and Matsushita the Examiner takes the position that:

> It would have been obvious....to modify the manufacturing process by the number of leads etched in Glenn, such that each lead is attached to two dies and then the sealing resin and a center line of each second metallic layer is cut in order to reduce cutting process time as taught by Matsushita.

## ARGUMENT

Appellant respectfully urges that claims 5, 6 and 8 patentably distinguish from the applied reference combination as the claimed subject matter would not have been obvious within the meaning of 35 U.S.C. §103(a).

In determining obviousness, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." (*Grain Processing v. American Maize*, 5 USPQ 2d 1788, 1793 (Fed. Cir. 1988))

In the present situation, it is submitted that rather than the combination of the prior art rendering obvious appellant's claimed invention as the Examiner purports, the prior art actually teaches against the manner in which the Examiner proposes to combine the teachings of the prior art.

It is submitted that if any of the references relied upon support a rejection under 35 U.S.C. §103 teach against the proposed modification, the prior art cannot "make obvious the invention," particularly when the proposed modification goes against the express teachings of the primary reference which is being modified.

While an Examiner can and should rely upon what the teachings of the references suggest, the Examiner cannot overlook or exclude from consideration what the references teach against.

If the proposed combination or modification destroys the teachings of one of the references relied upon, the combination is clearly improper. (See *Ex parte Hartmann*, 186 USPQ 366 (PTO Bd App 1974).

The Examiner has relied upon Glenn as disclosing:

...a method of manufacturing a plurality of semiconductor devices comprising steps of forming an electrodeposition frame (via etched metal; Par. 0037, 0038, Line 1) on a flexible substrate (10), said electrodeposition frame having first metallic layers (20) and second metallic layers (24) for external extension being patterned, wherein the first metallic layers are thicker than said second metallic layers so that the rear surfaces of the first and second metallic layers are flush with the bottom of the resin, contiguously mounting a semiconductor (28) with inherent electrode pads thereon said first metallic layers, wire bonding (29) the electrode pads to said second metallic layers, resin-sealing (30) said semiconductor element mounted on said electrodeposition frame is resin sealed with said semiconductor and using the substrate as a lower die, removing said substrate (Par 0053) to provide a resin sealing body; cutting said second metallic layers (Fig. 11, 13) and cutting a resin sealing body into individual semiconductor devices (Par 0056).

The Examiner concedes that "Glenn does not appear to disclose that said substrate is a metallic flexible substrate..." (emphasis added).

The Examiner has accordingly relied upon Jung et al. as utilizing "an inherently flexible metallic substrate (260)." (emphasis added).

In combining the teachings of Glenn and Jung et al. the Examiner takes the position that:

It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

In addition the Examiner states that:

Furthermore, it would have been obvious....to use metallic substrate as an alternate temporary substrate since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416 (1960).

It is important to fully consider the teachings of Glenn.

In paragraph 0004 Glenn introduces the invention in the context of disadvantages associated with the prior art by pointing out that the prior art has:

...foreseeable disadvantages. For example, the use of the metal temporary substrate and low-melting point alloy layer increase costs and manufacturing difficulty.

Thus, according to the teachings of Glenn, the prior art use of metallic substrates are associated with disadvantages that Glenn is concerned about overcoming and avoiding.

In paragraph 0006 Glenn discusses further disadvantages with the prior art stating:

First, the use of acid to dissolve the remainder of the copper plate after encapsulation creates a significant possibility of contamination, since such acids are generally regarded as dirty.

Again, Glenn indicates that the prior art use of metallic substrates requires the substrates to be removed by etching processes which produce contaminates that can adversely effect the resulting semiconductor devices.

In paragraph 0007 Glenn teaches that:

Accordingly, there is a need for a small and reliable package that is easier and less expensive to manufacture than prior art packages.

In paragraph 0010 Glenn teaches:

The present invention overcomes the disadvantages of the prior art by, among other things, the use of an inexpensive plastic sheet as a base for forming the packages

As a solution to the prior art use of metallic substrates and their associated disadvantages, Glenn purposely utilizes a plastic substrate having an adhesive surface which is exemplified by the use of adhesive tape in paragraph 0008.

The use of such a substrate allows Glenn to achieve a lower cost and a method of removing the substrate without exposing the packaged semiconductor device to potentially harmful etching solutions which are required to remove metallic substrates in the prior art.

It is accordingly submitted that Glenn's invention is directed to the use of a plastic substrate and the exclusion of metallic substrates in order to overcome the noted disadvantages of a metallic substrate.

The Examiner has conceded that Glenn fails to teach a metallic substrate.

Accordingly, the Examiner has relied upon Jung et al. as teaching the use of a metallic substrate 260.

As taught by Jung et al., substrate 260 is removed at the end of the fabrication process "utilizing an etching agent."

It is submitted that it would go against the express teachings of Glenn to modify Glenn to include the metallic substrate of Jung et al. as the Examiner suggests.

First, it is pointed out that the Examiner's proposed combination of Glenn and Jung et al. is improper under U.S. Patent Law because it is completely contrary to the express teachings of Glenn.

As held by the Patent Office Board of Appeals and Interferences in *Ex parte Hartmann*:

> References cannot properly be combined if effect would destroy invention on which one of reference patents is based. *Ex parte Hartmann*, 186 USPQ 366 (PTO Bd App 1974).

In response to the Examiner's stated basis that:

> It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

It is noted that Glenn teaches advantages associated with utilizing a plastic substrate over a metallic substrate.

Accordingly, plastic and metallic substrates cannot be considered equivalents or alternatives in the present situation. Glenn's choice of plastic substrates is not arbitrary, but rather based upon concrete disadvantages associated with metallic substrates and advantages associated with plastic substrates.

As held by the court of appeals in *In re Wesslau*:

> It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. *In re Wesslau*, 147 USPQ 391 (CCPA 1965).

Under this holding, the Examiner is required to fully consider the reasons as to why Glenn utilizes a plastic substrate and avoids the use of a metallic substrate.

When fully considering the teachings of Glenn, it becomes "obvious" that Glenn expressly avoids the use of a metallic substrate.

Accordingly, the express teachings of Glenn do not support the Examiner's position that:

> It would have been obvious....to form the substrate of Glenn as a metallic substrate as an alternative process in order to encapsulate a semiconductor chip with exposed leads.

The Examiner's second basis for modifying Glenn in view of Jung et al. was stated as follows:

> Furthermore, it would have been obvious....to use metallic substrate as an alternate temporary substrate since it has been held that to be within the general skill of a worker in the art to select known material on the basis of its suitability for intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416 (1960).

*In re Leshin* involves a situation in which the Board of Patent Appeals and Interferences upheld a rejection on the basis that:

> ...mere selection of known plastics to make container-dispenser of a type made of plastics prior to the invention, the selection of the plastics being on basis of suitability for intended use, is obvious.

In *In re Leshin* the prior art taught various plastic materials and the appellant argued that he "had to select them for his particular purpose" after conceding that the "the plastics he uses are well known"

In the present situation the Examiner is trying to apply the holding of *In re Leshin* to a situation in which the primary reference teaches a plastic substrate in order to overcome disadvantages associated with the prior art use of metallic substrates, and the secondary reference teaches a metallic substrate.

This is not a case of selective use of similar materials as in the case of *In re Leshin*. Moreover, Glenn expressly teaches functional differences and disadvantages associated with metallic substrates verses plastic substrates.

Therefore the holding in *In re Leshin* does not support the Examiners' stated position on obviousness and the Examiner's second basis for concluding that appellant's claimed invention is obvious over Glenn in view of Jung et al. is unfounded.

It is noted that in Glenn the lead frame and plastic substrate are attached to each other by an adhesive material. However, after attachment, peeling may occur which would allow the sealing resin to seep in between the lead frame and the plastic substrate. In such a case, the seeped in sealing resin cannot be removed and therefore poor conductivity may occur.

In contrast to Glenn, in the present invention the Ni (metallic layer) is formed by electrodeposition so that no gap is formed between the Ni layer and SUS. Therefore, the sealing resin cannot seep in between the Ni layer and SUS.

In Glenn the problem of the sealing resin seeping between the lead frame and plastic substrate can only be achieved by increasing the adhesive strength of the polyimide adhesive tape. This causes additional problems because after the plastic substrate is removed, the additional adhesive must also be removed. This adds an additional process step and increases costs.

The Examiner has relied upon Kweon et al. as teaching the use of deposited metallic thin film portions on first and second metallic layers that are exposed from a rear surface of a resin body.

In combining the teachings of Kweon et al. with those of Glenn and Jung et al. the Examiner states that:

> It would have been obvious....to deposit thin film portions of the first and second metallic payers that are exposed from a rear surface of said resin sealing body in order to provide electrical and mechanical connection as taught by Kweon.

The Examiner's further reliance upon Kweon et al. does not overcome the fact that the combination of Glenn and Jung et al. is improper under 35 U.S.C. §103.

The Examiner has relied upon Matsushita as disclosing cutting through a sealing resin and a centerline of second metallic layers.

The Examiner's further reliance upon Matsushita does not overcome the fact that the combination of Glenn and Jung et al. is improper under 35 U.S.C. §103.

In the Advisory Action of November 11, 2003 the Examiner has stated that:

...applicant has not provided extrinsic evidence that replacing the substrate of Glenn with another material will destroy the invention.

In response to the Examiner's position and suggestion for appellant to submit extrinsic evidence, a Declaration by Mr. KIMURA (unsigned) was being submitted under the provisions of 37 CFR §1.132.

The KIMURA Declaration provides a technical explanation from someone who is qualified as having ordinary skill in the art, as to the differences between applying metal layers on metal and plastic substrates and electrodeposition techniques for fabricating semiconductor devices.

The technical facts set forth in the KIMURA Declaration support appellant's position that it would not have been obvious to modify Glenn in a manner which involves substituting the plastic substrate of Glenn for the metal substrate of Jung et al.

From the facts in the KIMURA Declaration considered in light of the teachings of Glenn, one skilled in the art can readily conclude that Glenn does not teach electrodeposition at all, let alone forming an electrodeposition frame on a metal substrate.

Rather, Glenn teaches that "metal layer 16 may be applied by sputtering or chemical vapor deposition."

Moreover, Glenn does not recognize or appreciate, or is in any concerned with the differences in contact strength between metal layers on plastic substrates (deposited by sputtering or CVD techniques) and metal layers electrodeposited on metal substrates as explained in the KIMURA Declaration.

The Examiner's combination of the prior art is based upon the premise that there is no difference between using a plastic substrate in Glenn or modifying Glenn to have a metal substrate.

It is submitted that the facts in the KIMURA Declaration establish that there are significant differences between using a plastic substrate and a metal substrate in the fabrication of semiconductor devices.

Accordingly, it is submitted that the record, including the teachings of the prior art and the KIMURA Declaration, support appellant's position that the combination of Glenn and Jung et al. is not obvious under 35 U.S.C. §103, and that appellant's claimed invention is patentably distinguishable over the prior art.

It is noted that a signed copy of the KIMURA declaration will not be available until the second week of February. Accordingly, consideration of the technical facts presented in the KIMURA declaration is requested while arrangements are being made to submit a signed copy of the KIMURA declaration.

## CONCLUSION

For the reasons advanced above, appellant respectfully contends that the rejection of claims 5, 6 and 8 as being obvious under 35 U.S.C. §103(a) over Glenn. in view of Jung et al. and Kweon is improper because the examiner has not met the burden of establishing a *prima facie* case of obviousness.

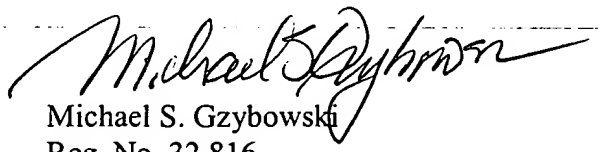
Moreover, for the reasons advanced above, appellant respectfully contends that the rejection of claim 7 as being obvious under 35 U.S.C. §103(a) over Glenn and Jung et al. and

further in view of Matsushita is improper because the examiner has not met the burden of establishing a *prima facie* case of obviousness.

Reversal of each of the rejections on appeal is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 CFR §1.136 is hereby made. Please charge the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 12-2136 and please credit any excess fees to such deposit account.

Respectfully submitted,



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## CLAIMS ON APPEAL

Claim 5. A method of manufacturing a semiconductor device comprising the steps of:

forming an electrodeposition frame on a flexible flat metallic substrate, said electrodeposition frame having first metallic layers and second metallic layers for external extension being patterned, wherein said first metallic layers are thicker than said second metallic layers;

contiguously mounting a plurality of semiconductor elements, each with electrode pads thereon, on said first metallic layers;

wire-bonding the electrode pads to said second metallic layers which are located between said semiconductor elements;

resin-sealing said semiconductor elements mounted on said electrodeposition frame;

removing said metallic substrate to provide a resin sealing body having a bottom so that rear surfaces of the first metallic layers and second metallic layers are flush with the bottom of said resin sealing body;

cutting said resin sealing body into individual semiconductor devices, wherein each device is provided with the first and second metallic layers; and

depositing metallic thin films on portions of the first and second metallic layers that are exposed at the bottom said resin sealing body.

Claim 6 A method of manufacturing a semiconductor device according to claim 5, further comprising after the step of cutting, the step of:

depositing metallic layers for electrodes to the second metallic layers exposed from a rear surface of said resin sealing body.

Claim 7 A method of manufacturing a semiconductor device according to claim 5, wherein

in said step of cutting of said resin sealing body, it is cut along a center line of each of the second metallic layers to provide metallic layers for external extension for adjacent semiconductor elements.

Claim 8 A method of manufacturing a semiconductor device according to claim 5, wherein said electrodeposition frame is resin sealed together with said semiconductor elements using said metallic substrate as a lower die.

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